



A rank-one Update Method for Efficient Processing of Interconnect Parasitics in Timing Analysis

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ABSTRACT

In this paper we present a rank-one update method for updating reduced-order models of interconnect parasitics when driver resistances or load capacitances change, as commonly occurs during timing analysis. These rank-one updates are extremely inexpensive, do not require reexamining the original interconnect network, and most importantly are *provably equivalent* to rereducing the original network. This abstract contains the proof only for the case of varying the driver resistance, but examples are given to show that the exactness holds more generally. In particular, a cross-talk case is examined where the conductance matrix is singular.

1. INTRODUCTION

The impact of interconnect delays on the performance of very high speed integrated circuits has made it necessary to adapt timing analysis tools so that interconnect delays are accurately modeled. In many of the gate-level timing analysis tools, the gates are presumed to be characterized by timing delays which are functions of gate load capacitance. Then, in an attempt to develop an accurate driver model to use while analyzing the parasitic components associated with the interconnect, most gate level tools convert the gate's timing information into a time-varying current source in parallel with a driver output resistor.

The difficulty with the above stated approach is that in order to determine the driver resistor, it is first necessary to determine the effective load capacitance on the gate. However, the effective load capacitance depends on the driver resistor, due to resistive shielding, and typically an iterative algorithm is used to arrive at a self-consistent solution [1]. The use of such an iterative algorithm requires reanalyzing the interconnect for many different driver resistances. In addition, the gate's driver resistor may also change under other circumstances. If the gate is complex, the output driver resistor may depend on what logic function is being performed, or may even depend on whether the gate's output is rising

or falling.

In order to improve the efficiency of the interconnect analysis, large networks of interconnect-related resistors, capacitors and inductors are usually reduced using numerical techniques that replace the original network with a low-order model that accurately represents both the delays and the loading effects. However, when these reduced-order models are going to be used in timing analysis, they are often more complicated because they must maintain accuracy over a wide range of possible gate driver resistances.

Although it is possible to rereduce the entire interconnect network every time the driver resistor changes, this has two distinct disadvantages. First, the reduction is computationally expensive. Second rereduction implies that all the parasitic networks for a given timing analysis must be stored for the entire analysis. In this paper we present an alternative based on performing rank-one updates of the existing reduced-order model. These rank-one updates are extremely inexpensive, do not require reexamining the original interconnect network, and most importantly are *provable equivalent* to rereducing the original network with the updated driver resistance. We start in the next section by briefly describing model-order reduction and then in Section 3 we give a circuit derivation of the rank-one update formulas for changes in both driver resistances and load capacitors. In Section 4, we give an outline of the proof that the rank-one updates are equivalent to rereduction for driver resistances. In Section 5, we show by example that the exactness holds more generally than there was space to prove in this short paper. We also demonstrate that the method can be used to easily handle a cross-talk case where the conductance matrix is singular. Conclusions are given in section 6.

2. BRIEF BACKGROUND ON MODEL REDUCTION

All the computational results below are for RC circuits, but the rank-one algorithm for updating reduced-order models seems, at least formally, to extend to RLC circuits. However, to simplify the exposition and to be consistent with our experiments, we consider just the RC case. If the drivers are represented using current sources entering at nodes 1 through m , the circuit can be converted to a system of differential equations using nodal analysis, in which case the system has the form

$$C\dot{v}(t) = Gv(t) + e_1u_1(t) + \dots + e_mu_m(t) \quad (1)$$

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where v is the n -length vector of time-varying node voltages, C and G are $n \times n$ nodal capacitance and conductance matrices, e_1, \dots, e_m are n -length unit vectors, and u_1, \dots, u_m are the time varying scalar input currents.

Since the first use of Krylov-subspace methods to compute reduced-order models of circuits [6, 4], variants of these methods have found wide acceptance due to their numerical robustness. Issues of stability and passivity have received considerable attention [2, 7], single-input multiple-output and multiple-input multiple-output approaches have been developed [8], and a projection framework for analyzing these methods has been carefully studied [9]. In this paper we will make extensive use of the recently developed PRIMA algorithm [10], so this algorithm will be briefly reviewed.

Although we will consider the multiple-input case experimentally, here we only consider the single input case, corresponding to assuming $m = 1$ in (1). This is a typical case, as often the parasitic networks in timing analysis have a single driver and multiple receivers. The PRIMA method for this single input case is based on separately projecting the C and G matrices in (1) using vectors generated from the Krylov-subspace

$$\{G^{-1}e_1, G^{-1}CG^{-1}e_1, \dots, (G^{-1}C)^{q-1}G^{-1}e_1\} \quad (2)$$

where q is the order of the model. Let V_q be the $n \times q$ matrix generated by sequential orthogonalization of the Krylov-subspace vectors, in which case the reduced-order model is given by

$$V_q^T C V_q \dot{z} = V_q^T G V_q z + V_q^T e_1 u(t). \quad (3)$$

or

$$C_r \dot{z} = G_r z + V_q^T e_1 u(t). \quad (4)$$

where z is the q -length state vector for the reduced-order model, $C_r = V_q^T C V_q$ and $G_r = V_q^T G V_q$ are $q \times q$ reduced matrices, and $V_q^T e_1$ is a q -length reduced input vector.

In a typical parasitic network, many of the node voltages will be outputs. Each of the output node voltages of interest can be related to the reduced-order model states using

$$\hat{v}_i \approx e_i^T V_q z \quad (5)$$

where \hat{v}_i is the reduced order approximation to node voltage v_i and $e_i^T V_q$ is the q -length row vector equal to the i^{th} row of V_q . It is perhaps instructive to consider how many floating point numbers are needed to completely describe the reduced order model. If there is one input, l outputs, and q states, then roughly

$$2 \cdot q^2 + (l + 1) \cdot q \quad (6)$$

floating point numbers are needed to represent the reduced-order model. Since q is typically less than five, once the q -th order model has been constructed, timing information is easily extracted by solving (4) using eigendecomposition or numerical integration.

3. A CIRCUIT-BASED DERIVATION OF THE RANK-ONE UPDATE FORMULAS

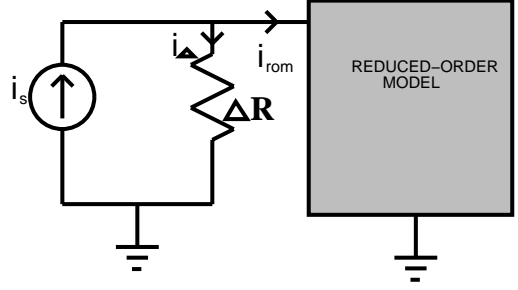


Figure 1: Circuit for deriving rank-one Update Formula

If the reduced-order model is extracted using a guess at the driver transistor's output resistor, the reduced-order model must be corrected every time the estimate of the driver resistor is updated. One approach to performing this update is to simply rereduce the original n -node parasitic network every time the driver resistor changes, but this is disadvantageous for two reasons. First, the reduction is computationally expensive. Second, and perhaps more importantly, such an approach implies that all the parasitic networks for a given timing analysis must be stored for the entire analysis.

A better approach would be to find some way of updating the reduced-order model directly, without going back to the original parasitic network. With such a method, the original large network could be reduced once, and then discarded. To see how to derive the update, consider the diagram in figure 1. In the diagram, ΔR is the change in the driver resistance, i_Δ is the current through ΔR , i_{rom} is the current entering the reduced-order model, and i_s is the driver current. The voltage across ΔR , denoted v_{in} , can be related to the reduced-order model states using (5). In particular,

$$v_{in} = (e_1^T V_q) z. \quad (7)$$

As i_{rom} is the input current to reduced-order model, the model's states satisfy

$$C_r \dot{z} = G_r z + V_q^T e_1 i_{rom}(t). \quad (8)$$

Summing currents and using the i-v relation for ΔR yields

$$i_{rom} = i_s - i_\Delta = i_s - \frac{v_{in}}{\Delta R} = i_s - \frac{1}{\Delta R} (e_1^T V_q) z. \quad (9)$$

Combining (7), (8), and (9)

$$C_r \dot{z} = G_r z - V_q^T e_1 \frac{1}{\Delta R} (e_1^T V_q) z + V_q^T e_1 i_s, = G_r^{updated} z + V_q^T e_1 i_s, \quad (10)$$

where

$$G_r^{updated} = G_r - \frac{1}{\Delta R} p_1 p_1^T \quad (11)$$

and p_1 is a q -length vector whose transpose is the first row of V_q .

The update to G_r , $\frac{1}{\Delta R} p_1 p_1^T$ is a $q \times q$ matrix whose columns are all scalings of the vector p . Updates of this form are often referred to as rank one updates.

It is also possible to derive an analogous formula to update any load capacitor, by following an analogous argument. The result is

$$C_r^{updated} = C_r + \Delta C p_j p_j^T \quad (12)$$

where ΔC is the change in the load capacitance at node j , and p_j is a q -length vector whose transpose is the j^{th} row of V_q .

4. AN EXACTNESS THEOREM

The rank-one update formulas derived in the previous section were based on simply combining the reduced-order model with external components to produce a combined model. What is surprising is that the drive resistor rank-one update formula produces EXACTLY the same reduced-order model as would be produced by rereducing the original n -node parasitic network from scratch, with the updated drive resistor. This surprising (at least to the authors) result follows from two facts. The first is a well-known property of rank-one updates, and the second is that the span of a Krylov subspace is invariant to certain rank-one updates of the associated matrix.

Below is a well-known property of rank-one updates [11]. If A is an $n \times n$ matrix and p is an n -length vector, then

$$(A + pp^T)^{-1} = A^{-1} + \alpha (A^{-1}p) (p^T A^{-1}) \quad (13)$$

where α is a scalar.

The following lemma is easily proved using (13).

LEMMA 1. For any vector u

$$(A + pp^T)^{-1}u = A^{-1}u + \beta A^{-1}p. \quad (14)$$

To prove the lemma, apply (13)

$$(A + pp^T)^{-1}u = A^{-1}u + \alpha (A^{-1}p) (p^T A^{-1})u. \quad (15)$$

Now let β be the scalar given by $\alpha p^T A^{-1}u$.

THEOREM 1. Let G^u be the $n \times n$ conductance matrix formed by updating the driver resistance and reapplying nodal analysis to the unreduced RC network. If V_q^u is the $n \times q$ matrix of Krylov-subspace vectors generated by sequential orthogonalization of

$$\{(G^u)^{-1}e_1, (G^u)^{-1}C(G^u)^{-1}e_1, \dots, ((G^u)^{-1}C)^{q-1}(G^u)^{-1}e_1\} \quad (16)$$

then

$$(V_q^u)^T G^u V_q^u = G_r^{updated} \quad \text{and} \quad (V_q^u)^T C V_q^u = C_r \quad (17)$$

where $G_r^{updated}$ are given in (11).

To prove the theorem, first note that when the drive resistor is updated only the first row and column of the $n \times n$ conductance matrix changes. In particular, the update to the conductance matrix is rank-one and is given by

$$G^u = G + \frac{1}{\Delta R} e_1 e_1^T. \quad (18)$$

Note that Lemma 1 and (18) can be used to show $G^{-1}e_1$ is parallel to $(G^u)^{-1}e_1$, and in addition it follows that

$$\begin{aligned} \text{span}\{G^{-1}e_1, G^{-1}CG^{-1}e_1, \dots, (G^{-1}C)^{q-1}G^{-1}e_1\} \\ = \text{span}\{(G^u)^{-1}e_1, (G^u)^{-1}C(G^u)^{-1}e_1, \dots, \\ ((G^u)^{-1}C)^{q-1}(G^u)^{-1}e_1\}. \end{aligned} \quad (19)$$

Since the two Krylov subspaces have the same span and parallel starting vectors, sequential orthogonalization will produce $V_q^u = V_q$ and

$$(V_q^u)^T C V_q^u = (V_q)^T C V_q. \quad (20)$$

Finally,

$$(V_q^u)^T (G + \frac{1}{\Delta R} e_1 e_1^T) V_q^u = V_q^T G V_q + \frac{1}{\Delta R} V_q^T e_1 e_1^T V_q \quad (21)$$

which is exactly the formula given in (11).

5. COMPUTATIONAL VERIFICATION

In this section we give several computational results to demonstrate the correctness of our theorem and to demonstrate that the rank-one updates have exactness properties beyond what was proved above.

The waveforms in Figure (2) are time waveforms for five nodes in an interconnect network with 463 resistors and 470 grounded capacitors. The results in the plot are the waveforms produced by the a rank-one updated reduced-order model and direct simulation of the entire circuit, notice they are very close to each other except for t close to zero. As is common for reduced-order models based on matching at $s = 0$, the initial dynamics have some small errors. In this example, the driver resistance update doubled the drive resistance. To experimentally validate our theorem, a fourth-order model was also generated by rereducing the original 933 element network with the updated driver resistor. The rereduced conductance and capacitance matrices were compared to the updated reduced conductance and capacitance matrices. The comparison was performed by comparing corresponding matrix elements, and the relative errors were less than 10^{-7} percent

The waveforms in Figure (3) are time waveforms for two nodes in a cross-talk example in which a driven RC line is capacitively coupled to two RC lines with no drive resistors. This problem is difficult to reduce because the conductance matrix is singular, and waveforms bear this out as one of them does not rise all the way to one volt. The rank-one approach solves this problem quite elegantly. A block Arnoldi method was used with three starting vectors, one corresponding to the driving point of each of the coupled RC lines. The initial reduction used finite drive resistors for all three lines, resulting in a nonsingular conductance matrix. Finally, the rank-one update formulas were used to effectively turn off two of the drivers, resulting in floating nodes. All though it is not clear from the plot, the waveforms from the direct simulation and rank-one updated reduced order model are in such close agreement that there appear to be only two node voltage waveforms.

6. CONCLUSIONS AND ACKNOWLEDGEMENTS

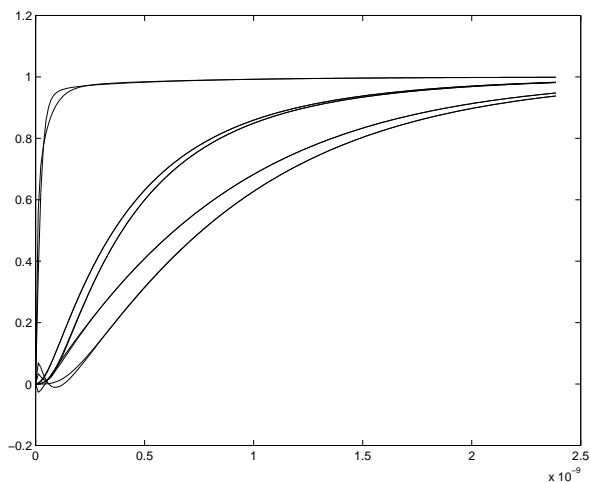


Figure 2: Comparison between 4-th order ROM and the direct simulation

In this paper we presented a rank-one update method for updating reduced-order models when drive resistances or load capacitances change. These rank-one updates are extremely inexpensive, do not require reexamining the original interconnect network, and most importantly are *provable equivalent* to rereducing the original network. Although we only proved the case for driver resistance changes, we showed by example that the exactness holds more generally by examining a cross-talk case where the conductance matrix is singular.

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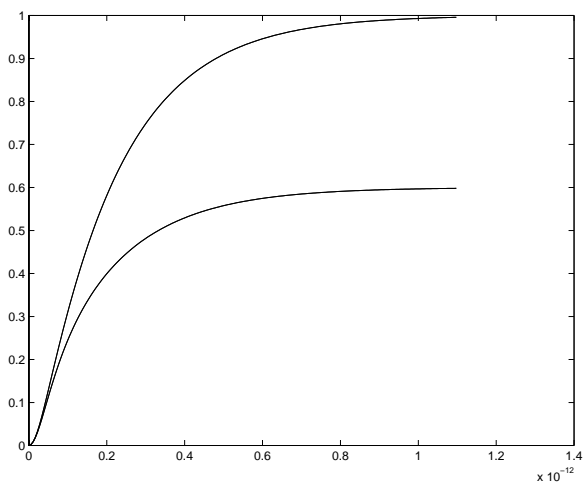


Figure 3: Two node voltage waveforms from a Cross-Talk Example. Update ROM results agree with direct simulation results to visual accuracy.

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