An RLC-line Reduction Algorithm with an Odd Optimality Property.

K. Nabors T.-T. Fang H.-W. Chang K. Kundert
Cadence Design Systems
San Jose, CA

J. White
MIT Department of EECS
Cambridge, MA 02139

1 Introduction

Timing verification tools must account for interconnect delay, and therefore require chip- or board-level RLC extraction. Such extraction can generate an enormous volume of data which is expensive to process. In order to reduce the data generated, as well as improve the efficiency of subsequent processing, "on-the-fly" reduction of RLC lines is typically performed. The most mature approach to RLC reduction are based on moment-matching procedures, as in [5, 6].

There are a variety of reasons for turning away from moment-matching procedures. If inductance is significant then the voltage waveforms are non-monotonic, and in that case matching ever higher moments may not be the best strategy [2]. In addition, the Padé approximates produced by the most common moment-matching procedures do not always preserve stability or passivity [4, 1, 3]. Finally, in many applications it is essential that RLC lines be reduced to RLC lines with fewer elements.

There are a number of effective algorithms for reducing RLC lines, see [3] for a survey. An approach with an odd optimality property can be derived using an observation in [7]. If the problem is an RLC line, then it is possible to specify the line by first defining the position, denoted R, along the RLC line as the total series resistance between the chosen position and the start of the line. Note, R varies between 0 and the total series resistance of the line. Then, the line can be completely specified by proscribing the capacitance c and inductance l as a function of R. For a distributed RLC line the $c(R)$ and $l(R)$ functions are continuous, and for a lumped line these functions can be represented using impulses. The problem of finding a small RLC circuit which matches an optimal number of moments in R can be recast into one which can be solved directly using Gaussian-quadrature [8].

[1] J. Eric Bracken. Passive Modeling of Linear Interconnect Networks. To appear, *IEEE Transactions on Circuits and Systems—I: Fundamental Theory and Applications.*

[2] Rohini Gupta, Seok-Yoon Kim, and Lawrence T. Pileggi. Domain characterization of transmission line models and analyses. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 15(2):184–193, February 1996.

[3] Andrew B. Kahng and Sudhakar Muddu. Efficient analyses and models of VLSI and MCM interconnects. personal note.

[4] Kevin J. Kerns, Ivan L. Wemple, and Andrew T. Yang. Stable and efficient reduction of substrate model networks using congruence transforms. In *IEEE/ACM International Conference on Computer Aided Design Digest of Technical Papers*, pages 207–214, 1995.

[5] Steven Paul McCormick. *Modeling and Simulation of VLSI Interconnections with Moments.* PhD thesis, Massachusetts Institute of Technology, June 1989.

[6] Lawrence T. Pillage and Ronald A. Roher. Asymptotic waveform evaluation for timing analysis. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 9(4):352–366, April 1990.

[7] E. N. Protonotarios and O. Wing. Theory of nonuniform RC lines, Part I: Analytic properties and realizability conditions in the frequency domain. *IEEE Transactions on Circuit Theory*, 14(1):2–12, March 1967.

[8] J. Stoer and R. Bulirsch. *Introduction to Numerical Analysis.* Springer-Verlag, New York, 1980.