A SCALABLE ROW/COLUMN-ADDRESSABLE DIELECTROPHORETIC CELL-TRAPPING ARRAY

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ABSTRACT
We present the first known implementation of a passive, scalable architecture for trapping, imaging, and sorting individual cells using a positive dielectrophoretic (p-DEP) trapping array. Our approach, which does not require on-chip CMOS electronics, incorporates unique "ring-dot" p-DEP trap geometries into an "active coverslip" array, enabling selection of individual cells from a trapped population. Interconnect demands for our design scale with the square root of the number of cells in the grid, which is a significant improvement over existing passive architectures. This technology aims to augment available microscopy techniques by enabling cell-based screens based upon imaged spatial and/or dynamic information.

KEYWORDS: row/column addressable, dielectrophoresis, single-cell manipulation, cell arrays

1. INTRODUCTION

Microscopy has enabled the visualization and analysis of numerous cellular and subcellular biological mechanisms, pathways, and processes. By imaging cells over space and time, many details pertinent to understanding cell function have been unveiled. Our work aims to enhance the capabilities offered by current optical techniques by offering a novel means for efficiently and viably sorting surveyed cells on the basis of visual and/or dynamic information (Figure 1). Such image-based sorting will empower new classes of cell-based genetic screens.

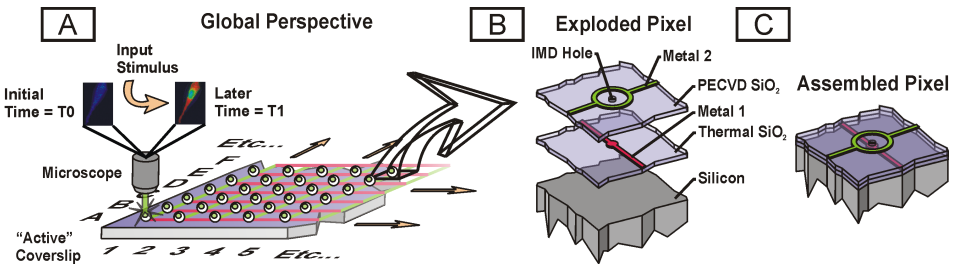

Figure 1: (A) *schematically outlines the overall functionality of the "active coverslip". Individual cells are held in specified locations on the trapping grid, interrogated using microscopy, and then sorted by grounding the associated row and column electrodes.* **(B)** *and* **(C)** *show exploded and assembled versions of an individual site in the overall trapping array indicating the two metal levels and their electrical isolation from one another. The intermetal-dielectric (IMD) hole permits electric-field communication between the two metal levels, enabling DEP trapping.*

2. SCALABLE ADDRESSING

To approach these types of cell-based screens we present a scalable "active coverslip" architecture affording single-cell manipulations. In our devices we organize collections of

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individually addressable DEP traps into row and column electrically connected arrays. This framework enables us to create a simple platform for trapping, imaging, and then selectively sorting many individual cells. While it is straightforward to create large arrays of DEP traps that are either all "on" or "off" [1], site-specific control is significantly more challenging. Existing approaches require either active CMOS-based architectures [2], with associated elaborate fabrication processes; distinct electrical connections for each trap, demanding at least *n* control lines for *n* traps [3, 4, 5]; or three-dimensional electrode configurations best suited for single cell translations rather than the removal of specific cells from a background population [6].

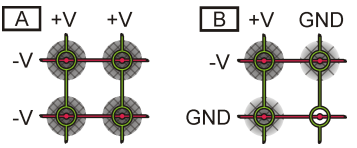

Figure 2: *Here we demonstrate the row/column addressing scheme.* **(A)** *shows a 2x2 grid where all sites are in the "on" state.* **(B)** *shows the same array with the lower right trap set to the "off" state. This condition is realized by grounding the associated row and column electrodes. Traps on the same row and column are "on" but activated with half the strength of other "on" state traps.*

Our addressing strategy, instead, uses a passive, transistor-independent selection approach where the addressed trap's associated row and column electrodes are grounded to free the held particle (Figure 2). The number of control lines for our scheme scales with the square root of the number of traps in the array. Thus, implementing 100×100 arrays capable of trapping enough cells for functional screens requires 200 chip-to-world electrical connections, rather than the minimum of 10,000 needed when scaling existing passive architectures.

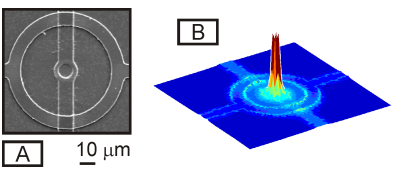

Figure 3: *Designing the "ring-dot" electrode configuration pictured in the SEM image in* **(A)** *involved substantial work using our modeling software [5].* **(B)** *indicates the effective DEP trapping force associated with the implemented design. The sharp peak in the central "dot" region shows high-strength force localization.*

3. FABRICATION

We create our sorting arrays on low-doped <100> silicon substrates using a two-level metal microfabrication process (Figure 1B). Thermally grown and patterned PECVD silicon dioxide layers provide electrical isolation between the aluminum conducting layers. Vias in the PECVD oxide layer enable electric-field communication between the two metal levels and DEP trap localization.

4. RESULTS

The key to our architecture is a unique "ring-dot" p-DEP electrode geometry (Figure 1C and Figure 3) organized in a row/column layout. We designed this "ring-dot" trap geometry using our previously reported quantitative modeling software (Figure 3B) [5] and have held particles against fluid flows on the order of 50-75 μL/min, affirming predictions. Our design's highly spatially localized DEP trapping fields enable single microparticle capture.

With both metal levels placed on the substrate of the device, our planar electrode format avoids any need for electrodes on the flow chamber ceiling. This feature, in contrast to many other prior designs [1, 2, 6], avoids placing additional restrictions on the permissible chamber heights used in our devices. Figure 4A-C highlights the row/column sorting

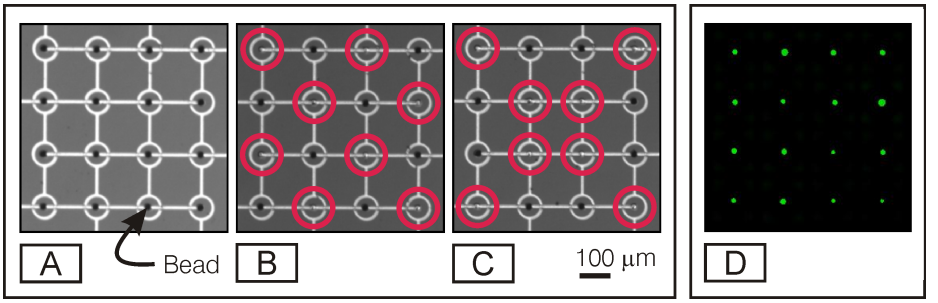

Figure 4: (A)-(C) *highlight row/column site release operations on a 4x4 p-DEP trap array.* **(A)** *displays the starting point for all addressing routines - all 16 sites are filled with single 20-µm diameter silver-coated polystyrene beads.* **(B)** *and* **(C)** *show examples of sorting patterns we can create by removing trapped particles using sequential selections. The white circles indicate locations where beads have been released.* ***(D)*** *provides a fluorescent microscopy image detailing trapping of HL60 cells in a 4x4 array. Each site holds just one cell, demonstrating single-cell trapping.*

capabilities of the device by presenting images of a simple 4×4 array where we have selectively released silver-coated polystyrene beads from an initially full grid to form arbitrary patterns. Further functionality is shown in Figure 4D where individual HL60 cells are positioned in a 16-site array.

5. CONCLUSIONS

Our strong planar DEP traps, structured in an addressable row/column architecture, offer a unique and easily scaled method for positioning and manipulating many individual cells. With this technology, we aim to add breadth to the suite of investigative tools available to biologists by providing a route toward cell-based genetic screens where sorting is based on imaged spatial and/or dynamic cues.

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